UC National Laboratory Fees Research Program – 2024 Workshop

Research Advancing Microelectronics: Workshop Report

The UC National Laboratory Fees Research Program (LFRP) sponsored a workshop series to advance innovative research and strengthen collaborations between the University of California (UC) and the (UC) national laboratories, in the field of research advancing microelectronics. Participation was open to researchers at the ten UC campuses and the three UC-affiliated national laboratories (Lawrence Livermore, Los Alamos, and Lawrence Berkeley National Laboratories).

Workshop Convenings

The workshop series consisted of two full-day hybrid convenings on the following dates:

- January 19, 2024, University of California Livermore Collaboration Center (UCLCC)
- January 30, 2024, Qualcomm Institute, UC San Diego

Each convening consisted of presentations from UC and national laboratory leadership that highlighted the current challenges in the field of microelectronics, and resources for collaboration across UC and the national laboratories. The workshops also included working group break-out sessions in which participants identified specific opportunities for UC-national lab collaborations that are advantageous and ground-breaking.

Workshop Report

The attached workshop report presents the content of the workshop series, from the high-level overview from UC leadership on the state of the field and the current challenges, to the research priorities identified by each breakout group. The report also provides an overview of the facilities and capabilities of the UC and the three UC-affiliated national labs in the area of microelectronics, as well as their ongoing regional and national collaborations in this field. The report lays out considerations for institutions and individuals alike in expanding engagement between UC and the national labs and deepening existing partnerships. Finally, the report identifies potential for engagement of early career scientists, postdoctoral researchers, and UC graduate and undergraduate students.

The report is publicly available and is intended as a resource to inform and support research UC-national lab collaborations, including identifying promising avenues of research and relevant facilities. Individuals applying to the UC Multicampus-National Laboratory Collaborative Research and Training (CRT) Awards competition for 2025 are encouraged to consult the report. Applicants should adhere to the program priorities, guidelines and policies outlined in the LFRP CRT Request for Proposals.

Workshop Title: Research Advancing Microelectronics
Host/Coordinating Institution: UC Davis
Workshop PI Name: Davis, Cristina
Workshop Report Authors: Davis, C., Cordova, A.L., Islam, S., Seker, E. [UC Davis]; Erpebeck, H., Rondinone, A. [LANL]; Shalf, J., La Fontaine, B., Johansen, W., Yao, Z. [LBNL]; Kotovsky, J., Haque, R., Schweickert, M., Nikolic, R., Schwegler, E., Beck, K., Voss, L. [LLNL]; Cybart, S., Lake, R., Wang, A., Tan, S. [UCR]; Asbeck, P., Lo, Y., Rao, R. [UCSD]; Fischer, P. [UCSC/LBNL]; Cabric, D. [UCLA].

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Executive Summary

The UC National Laboratory Fees Research Program (LFRP) designed a workshop series to advance innovative research and strengthen collaborations between the University of California (UC) and the (UC-affiliated) National Laboratories. The two workshops were jointly led by UC and National Laboratory teams and were open to faculty, research scientists, and postdoctoral fellows from all UC locations, including the ten campuses, and Los Alamos, Lawrence Livermore, and Lawrence Berkeley National Laboratories. The workshops' goal was to articulate a roadmap for advancing the field and to establish a foundation for future partnered research across the UC campuses. The workshop series consisted of two meetings – one at the University of California Livermore Collaboration Center and the second at the California Institute for Telecommunications and Information Technology (CALIT2) Qualcomm Institute on the UC San Diego campus. The sessions included keynote presentations, tours and working group break-out sessions to identify areas in which the UC National Laboratory collaborations are advantageous and ground-breaking. The workshops were also structured to provide networking opportunities to foster new partnerships between UC and UC National Laboratory researchers.

The following report highlights the discussions that took place at the workshops and the outcomes in order to guide UC's strategic investments into research advancing microelectronics, including research in materials, devices, and computing to advance the development of cutting-edge microelectronics.

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Background and Current Status

PURPOSE AND GOALS

The semiconductor industry has been improving and advancing technology at an exponential pace, driven by Moore's law. The strategic importance of microelectronics stems from its indispensable role in driving economic prosperity, safeguarding national security, fostering technological leadership, ensuring supply chain resilience, accelerating innovation, and creating high-value jobs. Collaborative efforts between government, industry, academia, and other stakeholders are essential for addressing the talent gaps and advancing the microelectronics agenda to secure a prosperous future.

The LFRP Microelectronics Workshops aimed to facilitate collaboration and research partnerships between the University of California and the National Laboratories, specifically focusing on semiconductor and microelectronics research. It served as a platform to address challenges and opportunities in this field by leveraging the strengths of the UCs and the National Laboratories.

The primary goal of the workshops and upcoming LFRP solicitation is to create long-term sustained collaborations in groundbreaking microelectronics research areas that are mutually beneficial and strategically important to UCs, National Laboratories, the State of California, and the nation. These collaborations are intended to be competitive nationally and internationally, aiming to create teams that become global leaders in microelectronics research.

Additionally, the workshops laid the groundwork for future partnered research endeavors while broadening participation and providing training and career opportunities for graduate students, postdocs, early career faculty, and new National Laboratory scientists. This initiative aligns with the broader goal of workforce development and nurturing the pipeline for the National Laboratories.

Furthermore, the workshops provided a blueprint for future and more frequent networking opportunities for potential collaborators and to find new research avenues. Participants had an opportunity to dive deeper into the topic of microelectronics and articulate a roadmap to advance the field. These workshops identified key opportunities for UC - National Laboratories collaborations that leverage the complementary strengths, resources and facilities of both entities.

Challenges and Opportunities in Microelectronics Research

The keynote speakers, UC San Diego Dean of Engineering Albert Pisano and UC Berkeley Dean of Engineering Tsu-Jae King Liu provided plenary presentations that shed light on the prevailing challenges and opportunities within the microelectronics and semiconductor research domain. Both speakers underscored the importance of action beyond the CHIPS Act, emphasizing the pivotal roles of National Laboratories and UC research programs in propelling semiconductor innovation forward. Emphasizing the necessity of ongoing investment in research and development, they highlighted the potential for advancements in transistor design and memory technology to revolutionize performance and efficiency across various technologies and applications. Furthermore, they stressed the significance of exploring alternatives to conventional silicon computing models and the importance of aligning research efforts with market trends to effectively scale innovations and meet burgeoning demands. Highlighting the symbiotic relationship between silicon and emerging technologies, they articulated a vision aimed at fostering technological advancement in device scaling, materials

innovation, and energy-efficiency to address the formidable challenges posed by escalating manufacturing costs and energy consumption.

Some of the specific opportunities for LFRP investment identified during the workshops include:

- **Novel Materials and Devices**: Exploring alternative device technologies beyond traditional CMOS transistors could open up new avenues for innovation. This may include research into quantum devices, photonics, spintronics, and ferroelectric devices to enhance the performance of integrated systems.
- **Co-Design of Future Systems**: With the traditional approach of scaling transistors reaching its limits, there is a need for co-design of future systems and co-innovation across the entire technology stack. This approach involves collaboration between application developers and technology designers to optimize energy efficiency and minimize costs for specific applications.
- **Enhanced CMOS and Integration**: Explore enhanced CMOS technologies and investigate integration techniques such as 2.5D and 3D integration. Research could focus on developing novel fabrication processes, materials, and design methodologies to enhance performance, reduce power consumption, and enable new functionalities in integrated circuits such as compute-in-memory.
- **Advanced Packaging Technologies**: As the cost of manufacturing chips increases, there is a growing focus on advanced packaging technologies to maximize interconnection density and minimize the interconnection distance between chips. Research in this area can lead to innovations in stacking chips on top of each other, thereby improving overall system performance and efficiency.
- **Energy Efficiency in Computing**: There is a significant opportunity for research aimed at improving the energy efficiency of computing devices. This could involve developing new materials, devices, and architectures such as neuromorphic or quantum, tailored for specific applications to maximize energy efficiency.
- **Green Manufacturing:** Research is needed to address environmental challenges associated with semiconductor manufacturing, such as reducing emissions and waste. This includes developing greener fabrication processes, minimizing the use of harmful chemicals, and improving overall manufacturing efficiency.
- **Edge Computing:** Explore further advancements in edge computing technologies, including investigating methods to optimize cost, energy consumption, reliability, security, and personalization, as outlined by Intel and Qualcomm's laws of edge computing. Edge computing presents opportunities for innovation in transistor design. As edge computing relies on distributed processing closer to the data source, there is a need for efficient and low-power transistors to support these systems.
- **Alternative Computing Models**: Investigate computing models beyond traditional silicon, considering emerging paradigms like mobile architecture. Research could focus on developing technologies that enhance the efficiency, scalability, and versatility of computing systems for mobile and edge applications.

- **Syndicated Fabrication Models**: Conduct research on syndicated fabrication models to facilitate rapid prototyping and innovation in transistor and memory technologies, and agile responses in semiconductor development. Explore methods to leverage existing infrastructure and collaborative networks of specialized fabrication facilities to accelerate innovation and reduce time-to-market for semiconductor products.
- **Sensor Integration and Communication**: Investigate methods to integrate sensors, processing, and communication into single modules, focusing on reducing form factor, power consumption, and cost while enhancing functionality and performance. Research could include developing innovative sensor technologies, communication protocols, and system architectures for diverse applications ranging from IoT to healthcare. This integration could lead to novel transistor and memory designs optimized for specific applications, such as edge computing or IoT devices.
- **Antenna Technologies:** Research in advanced antenna technologies for wireless communication, including flip chip antennas and beamforming antennas. Explore novel antenna designs, materials, and integration techniques to improve efficiency, range, and reliability in wireless communication systems.
- **Application-Specific Memory Solutions**: With the growing demand for specialized computing solutions (e.g., AI, IoT), there are opportunities to develop application-specific memory solutions tailored to the unique requirements of these applications. This could involve optimizing memory architectures for specific workloads or implementing novel memory technologies to improve performance and energy efficiency.
- **Optical Communication:** Investigate emerging optical communication technologies for high-speed data transmission and networking. Research could focus on developing solid-state steerable lasers, optical beamforming techniques, and multiplexing methods to enhance bandwidth, reduce latency, and improve scalability in optical communication systems.
- **Human-Machine Interaction**: Explore human-machine interaction technologies, including methods for intuitive and seamless interaction with computing devices. Research could include developing novel input/output modalities, user interfaces, and interaction techniques to enhance user experience and productivity in diverse computing environments.
- **Workforce Development**: Research into effective methods for workforce development, such as training programs for technicians and collaboration between academia, industry, and National Labs, is crucial to address talent shortages in the semiconductor industry. Collaborative teaching agreements between research institutions and National Labs can facilitate knowledge exchange and inspire students to pursue careers in semiconductor technology. Dual appointments, where researchers split their time between the lab and academia, can also help foster direct interactions with students and facilitate internships and permanent positions in research institutions.

These research areas align with the overarching aim of fostering innovation in semiconductor and microelectronics technology and its associated domains, offering opportunities that extend across various sectors such as consumer electronics, telecommunications, healthcare, automotive, and

beyond, while simultaneously tackling issues concerning energy efficiency, environmental sustainability, and cultivating a talent pipeline.

Importance of Collaborations in the Path of Science and Discovery

UC President Emeritus Robert Dynes' plenary session at UC San Diego underscored the vital role of collaborative relationships between academia, National Laboratories, and industry in advancing scientific research and technological innovation. He highlighted historical partnerships, spawned by researchers at the University of California and the University of Chicago, that resulted in the establishment of Lawrence Berkeley and Los Alamos National Laboratories. He underscored their ongoing relevance in addressing contemporary challenges like microelectronics and information management. He noted that a willingness to go wrong in pursuit of hard questions was essential for driving innovation and maintaining national leadership in scientific research. Reflecting on the evolution of Moore's Law, President Dynes emphasized the criticality of collaborations across the seams between industry, National Laboratories, and academia in pushing the boundaries of technological advancement, including exploring emerging fields like quantum computing. He encouraged a forward-thinking approach to research and emphasized the importance of interactions between lab researchers, faculty and students to spur new ideas and breakthroughs. He noted that the labs have numerous resources that are difficult to find when faculty seek collaboration. He encouraged faculty to contact National Lab outreach administrators for guidance in finding co-aligned lab researchers for collaborative projects.

CURRENT ACTIVITIES AND CAPABILITIES

UC campuses and National Laboratories have long collaborated on groundbreaking research initiatives, spanning a diverse array of fields including microelectronics and semiconductors. Although an exhaustive catalog of their joint efforts would be challenging to compile, several recent and pertinent multi-institutional programs stand out. These collaborations often leverage the complementary expertise of UC campuses and National Laboratories, fostering innovation and pushing the boundaries of scientific inquiry. These joint endeavors exemplify the power of partnership in addressing pressing global challenges and driving scientific progress forward.

The **California Pacific Northwest AI Hardware Hub**, co-led by UC Berkeley and Stanford, with UC Davis as a core partner primarily for workforce development and Lawrence Livermore National Laboratory as a fab facility partner, is an initiative aimed to drive collaboration and innovation in the field of microelectronics and artificial intelligence hardware. With over 40 academic institutions, National Laboratories, and industry partners, the hub covers the entire semiconductor value chain, from materials and devices to EDA and chip design, packaging and system prototyping and testing. Using a lab-to-fab translation model, the hub provides infrastructure and expertise to bridge the gap between research and high-volume manufacturing. This is crucial for scaling up academic innovations for commercial deployment. Additionally, the hub runs a program to educate and train students from Community Colleges in microelectronics, fostering workforce development to support the local semiconductor industry.

The **California Defense Ready Electronics and Microdevices Superhub (California DREAMS)** in Southern California is one of the eight microelectronics technology hubs supported by DoD under the CHIPS Act. It unites five UC campuses (Los Angeles, Irvine, Riverside, Santa Barbara, and San Diego), industries in southern California, and organizations from the East Coast to form a consortium and pursue microelectronic research. The hub accelerates developing, prototyping, and adopting advanced RF and supporting technologies for 5G/6G applications. The hub is creating a syndicated fabrication model, leveraging resources like the metal oxide semiconductor implementation service (MOSIS) and a network of specialized foundries for rapid prototyping and integration for processes in University and industrial labs. This agile approach allows for quick iteration and identification of future manufacturing needs. Additionally, the hub explores innovative solutions like flip-chip antennas and beamforming technology to meet evolving data transmission demands, ensuring its relevance in the rapidly changing landscape of microelectronics. The California DREAMS team leads the compound semiconductor industry, specializing in GaAs, GAN, InP, and more. With a focus on supporting the Department of Defense's 5G/6G needs, the California DREAMS is committed to training the next generation of microelectronics engineers and seeks to increase the number of advanced degrees in radio frequency engineering.

Additionally, each UC campus has facilities that can be leveraged in multi-campus, multi-PI efforts and research. The table below highlights some of the facilities across the UC system:

UC Campus	**Relevant Facilities**
UC Berkeley	Marvell Nanofabrication Laboratory
UC Davis	Center for Nano-MicroManufacturing (CNM2) Advanced Materials Characterization and Testing Laboratory (AMCaT) Davis Millimeter Wave Research (DMRC) GEM5 Architectural Simulator Lead
UC Irvine	California Institute for Telecommunications and Technology (Calit2) UC Irvine Materials Research Institute (UC IMRI) Integrated Nanosystems Research Facility (INRF)
UC Los Angeles	CHIPS Lab UCLA Nanofabrication Laboratory (NanoLab) Center for High Frequency Electronics (CHFE)
UC Merced	The Stem Cell Instrumentation Foundry, featuring a class 100/1000 cleanroom for microfabrication. The Imaging and Microscopy Facility The NSF MRI-funded Pinnacles and MERCED computer clusters

UC Riverside	California Institute for Telecommunications and Technology (Calit2) Center for Nanoscale Science & Engineering Nano-Fabrication and Electron Microscopy Facility (NFEM) Center for Superconductive Quantum Electronics (CSQE) UC System-wide Center for Ubiquitous Communication by Light (UC-Light) Laboratory for Integrated Circuits and Systems (LICS)
UC Santa Barbara	UCSB Nanofab
UC San Diego	Qualcomm Institute Nano3 Cleanroom Facility (Nano3) Qualcomm Institute Circuits Lab Qualcomm Institute Chip-scale Photonics Testing Qualcomm Institute Prototyping Facility and Design Studio San Diego Supercomputing Center (SDSC)
UC Santa Cruz	Materials Science & Engineering Initiative (MSEI) Santa Cruz Institute for Particle Physics Radiological Instrumentation Laboratory W. M. Keck Center for Nanoscale Optofluidics

THE NATIONAL LABORATORIES

Los Alamos National Laboratory (LANL) is a multipurpose National Nuclear Security Administration lab with significant footprints in physics, materials science, computational science, manufacturing science, theory and modeling. Major user facilities include the Center for Integrated Nanotechnologies (CINT), the National High Magnetic Field Laboratory Pulsed Field Facility, and the Los Alamos Neutron Science Center. LANL hosts approximately 2000 students per year, with a mix of undergraduate (summer) and graduate (semester and full-time resident) students. Major research facilities may be found here: Science Facilities | Los Alamos National Laboratory (lanl.gov). LANL has advanced capabilities for electronic and quantum materials synthesis, architecture development, nano and microfabrication (through CINT), quantum computing, high performance computing, and characterization of both materials structure and function. LANL also hosts the Ion Beam Materials Laboratory which provides nine end-stations across three accelerators, capable of implanting most of the periodic chart at energies from kV to MV, at wafer scale.

LANL currently engages in a wide range of microelectronics research. Of CINT's 366 publications in CY2023, approximately 25% were in microelectronics materials (or closely related quantum materials) theory, device performance, or fabrication science. CINT hosts a best-in-class research grade cleanroom and over a dozen techniques for thin-film deposition, ranging from molecular-beam epitaxy (III-V from infrared to ultraviolet), physical vapor deposition, chemical vapor deposition, Si/Ge structure growth within situ doping, and pulsed laser deposition (for materials including actinides). The High Magnetic Field Laboratory engages in quantum and microelectronic materials research using a suite of high speed, high field pulsed techniques to understand magnetic

and electronic structure. The Ion Beam Materials Laboratory produces a wide range of doped electronic materials for both internal LANL users and CINT users. (CINT.LANL.GOV)

The LANL Computer, Computational and Statistical Sciences Division (CCS) conducts research in advanced architecture, neuromorphic simulation, and design. CCS leads the way for scientific applications at extreme scale through co-design of algorithms, programming models, system software, and tools. CCS scientists explore new programming models, data-intensive computing, data science at extreme scales, and application and algorithm co-design. The Intelligence and Space Research Division has interests in radiation tolerance of microelectronics and the MPA-Quantum group conducts research in quantum materials and devices.

Lawrence Livermore National Laboratory (LLNL) is known for groundbreaking research in nuclear science, high performance-computing, laser sciences, advanced sensing, biotechnology and more. Our work strengthens US security with world-class science, technology and engineering and multidisciplinary partnerships with academia and industry. Our staff enjoy working with academic partners through joint appointments, welcoming faculty on sabbatical and co-mentoring students throughout their research programs. LLNL hosts approximately 1000 students per year, including opportunities across education levels (community college, undergraduate, and graduate) and programs designed to inspire workforce diversity and inclusion.

The Center for Micro and Nano Technologies (CMNT, https://virtualtours.llnl.gov/facilities/cmnt/) at LLNL is a multi-user, multi-programmatic facility that houses a state-of-the-art cleanroom with broad semiconductor device capabilities with a focus on processing of micro and nanoscale structures and cutting-edge research and development. The fully capable facility maintains extensive lithography, etch, deposition, growth, packaging, test and characterization facilities. The facility strives to enable new architectures and materials and accommodates bold material permissions to create next generation devices for internal and external partners. The cleanroom also features a biomedical microfabrication foundry, a toolset for the design, fabrication, packaging, integration, and characterization of human-use implantable medical devices.

Beyond this specific facility, there are a multitude of other LLNL capabilities and centers that are relevant to advancing microelectronics research. LLNL's institutes and centers provide pathways to collaboration with the academic community (https://st.llnl.gov/partnerships/LLNL-Institutes-Centers). These entities develop strategic partnerships with universities around the world, fostering research excellence and serving as a training ground for undergraduates, graduate students, and postdoctoral fellows, some of whom will join Laboratory's workforce of scientists and engineers. Livermore Valley Open Campus (LVOC) is designed to facilitate improved interaction with outside organizations. The LVOC includes our Advanced Manufacturing Laboratory to allow LLNL to partner to develop tools and processes to address manufacturing challenges (https://engineering.llnl.gov/collaboration/aml). LLNL's Quantum Design and Integration Testbed (QuDIT, https://quantum.llnl.gov/) is a state-of-the-art facility for superconducting device testing and quantum information science research and houses two 10mK dilution refrigerators with control electronics for characterization and qubit operation as well as optical fiber connections. LLNL computer facilities include high performance novel AI accelerators that can apply energy efficient AI and ML techniques to scientific problems such as materials design and additive manufacturing. SambaNova DataScale and the Cerebras wafer-scale integration systems enable AI and ML offload to HPC clusters. The Nondestructive Characterization Institute (NCI, https://nci.llnl.gov/) is capable of cutting-edge micro and nanoscale nondestructive evaluation

approaches, with a focus on measuring quantitative internal physical properties of materials, components, and systems without causing damage. The Center for Accelerator Mass Spectrometry (CAMS, https://cams.llnl.gov/) focuses on ion-beam analytical techniques with three accelerators onsite. LLNL is also home to the MegaJOuLe Neutron Imaging Radiography (MJOLNIR) facility, which is a prototype neutron source for dynamic flash neutron radiography. It is capable of capturing neutron images on a very short (~50 ns) time frame and also has a time-gated neutron camera and several neutron time-of-flight diagnostics. Finally, our National Ignition Facility (NIF, https://lasers.llnl.gov/) continues to respond to national security needs and basic science work that only this facility can. Beyond the multitude of high-energy density physics programs made possible by NIF, it also serves to deliver neutron dose rates of electronic and other devices at fluences found nowhere else on earth.

Lawrence Berkeley National Laboratory (LBNL) microelectronics researchers follow a co-design approach to furthering microelectronics science, from atoms to architecture. The idea is to use theory and modeling in combination with design and prototyping, as well as characterization to advance the science of microelectronics, while leveraging state-of-the-art capabilities. DOE funded user facilities at LBNL include the Advanced Light Source, the Molecular Foundry, and NERSC. The Center for X-Ray Optics (CXRO) operates a suite of facilities, e.g. MET5 that are highly relevant to ME research. LBNL is also a leader in virtual prototyping capabilities such as the Materials project and ARTEMIS/FerroX which are enablers for existing microelectronics projects and programs. Current programmatic activities include the Center for High-Precision Patterning Science (CHiPPS), the co-design of ultra-low voltage beyond Moore, the co-design and integration of nano sensors on CMOS, as well as several core program activities related to ME, such as the Quantum materials, the Non-equilibrium magnetic materials, the van der Waals heterostructures, and the Electronic materials programs. Those world leading activities and capabilities offer opportunities for extensive collaborations across National Labs and UC campuses, including student internships, with a focus on increasing diversity, equity and inclusiveness. Information about these projects and capabilities, along with contacts, can be found on the following URLs: https://www.lbl.gov/research/microelectronics-and-beyond/ and https://materialssciences.lbl.gov/

SUMMARY OF BREAKOUT SESSIONS

The initial workshop series launched in Fall 2023, and was focused on research advancing microelectronics, including research in materials, devices, and computing to advance the development of cutting-edge microelectronics. Breakout sessions were organized around applications and technologies, while encompassing discussion in materials, devices and computing. The following areas of research in microelectronics discuss potential UC and National Laboratory collaborations, and of strategic value in advancing the field of microelectronics (in no particular order):

1. **MEMS and Sensors.** MEMS (MicroElectroMechanical Systems) technology enables the creation of miniature mechanical, electromechanical, and electrochemical devices akin to VLSI circuits. It's a microelectronics subfield focusing on integrating small-scale mechanical devices into electronic systems using techniques like photolithography. MEMS development has gained importance, yielding micrometer-sized devices with mechanical and electrical components. Sensors are

ubiquitous in many sectors and applications that span automotive, communications, and health care. Micro-electro-mechanical systems (MEMS), enabled by the very microfabrication technology for building integrated circuits, play an integral part in many of the sensors as well as in actuators (e.g., inkjet printer nozzles). Utilizing mature semiconductor processes, MEMS devices boast high reliability. Their compact size, low power consumption, and high performance render them ideal for optical switches.

2. **Electronics and Photonics for Extreme Environments.** Crucial for the safety and performance of key industries, including sectors like power and energy distribution (smart grids), gas, oil, and geothermal energy exploration, tough industrial processes, transport on land, in air, space, and deep space, as well as nuclear power plants.
3. **Packaging, Heterogeneous Integration and Design-for-Reliability.** Heterogeneous integration is a key technology that allows monolithic integration of different devices in dissimilar materials built in different technologies delivering the best functionalities in their native devices with advanced Si IC chips. Advanced packaging technologies are critical to achieving the highest microsystem performance enabled by HI. Furthermore, performance and reliability are the two core attributes of any IC chips and microelectronics system products. Understanding reliability issues and providing robust design-for-reliability (DfR) solutions are critical research tasks in developing any microelectronics products at all levels. DfR research becomes extremely challenging at advanced IC technology nodes, for hetero-integrated microsystems and for advanced packaging, which requires multi/inter-disciplinary research collaboration and cross-boundary holistic design methodologies.
4. **Modeling and Simulation.** Modeling and simulation play an important role in the R&D of microelectronic devices as it provides a “virtual prototyping” facility to evaluate many different design options before the costly process of actually synthesizing the materials or building the devices has commenced. In so doing, a very broad design space of potential realizations of an advanced microelectronics device or material, or architecture can be evaluated for its performance potential before it is ever built.
5. **Quantum Devices.** Quantum devices include and represent a broad range of novel physical hardware systems that will enable computations that are currently impossible or impractical to perform on classical hardware. Furthermore, quantum electronics offer a pathway to energy efficient computational systems.
6. **Wireless:** Critical technical challenges facing the wireless area and possible methods of addressing them were discussed. Growth rate of wireless data rate over the past 25 years has been more rapid than Moore’s Law; the number of global mobile subscribers now exceeds the population of the planet; a new wave of explosive growth is imminent, with the Internet of Things. Key challenges include 1) finite RF spectrum; 2) finite power per user; 3) interference and security problems; 4) development for specific application issues. Key areas of research identified were 1) heterointegration and advanced packaging; 2) modeling and simulation of complex 3D systems; 3) ultra lowultralow power sensors; 4) biomedical and wearable electronics; 5) high frequency device; 6) and circuit characterization digital predistortion and correction.
7. **NextGen Electronic Materials and Devices.** Future microelectronics will rely heavily on our ability to explore new approaches to further miniaturize components and to move information between different parts of a computer chip at high speed, and most importantly requiring orders of magnitude lower power than what is available today. An accelerated discovery and development of the next

generation of electronics materials and devices is of paramount importance, but we need to also recognize economic viability, environmental sustainability, and national security aspects. A complementary or enhanced technology was discussed in the form of neuromorphic devices and computers. These structures more closely mimic the architecture of the human brain and are not subject to the limits of Moore's Law. The logic is not digital and results in probabilistic conclusions. Applying these geometries results in a million (10**6) times less energy consumption than digital semiconductor logic.

8. **Electronic Design Automation:** EDA solutions are essential in chip manufacturing despite not directly manufacturing chips. They serve many crucial functions. In Technology Computer-Aided Design (TCAD), they aid in designing and validating semiconductor manufacturing processes for optimal performance and density. They provide the synthesis flow from high level design concepts like algorithms to physical layouts suitable for manufactures. Emphasis was first placed on fostering a skilled workforce from universities to contribute to the development of EDA tools, spanning traditional CMOS flow using open-source platforms like OpenROAD and extending to merging beyond-Moore devices. Proposed collaborative projects also include ML/AI enabled fast simulation and compact modeling using physics-informed neural networks (PINN) at various levels (from devices/TCAD, circuits and system levels) and automation for optimal processes to calibrate reduced/compact models.

Several **cross-cutting themes** were identified across several breakout sessions:

- Supporting education and **workforce development;**
- **Modeling and simulation** (virtual prototyping) codes and organizing cross-UC access to computing capabilities;
- Organizing **access to facilities** to prototyping capabilities and facilities that are distributed across the UC complex.

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Breakout Session Findings and Recommendations

The following section summarizes the discussion that took place over eight breakout sessions where UC and National Laboratory scientists provided presentations and identified key areas for research and partnership. The organizing committee thanks volunteer moderators who guided the conversations and provided summaries that are incorporated into this report.

MEMS & Sensors

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Razi Haque, Group Leader, Implantable Microsystems, Lawrence Livermore National Laboratory

Sensors are ubiquitous in many sectors and applications that span automotive, communications, and health care. Micro-electro-mechanical systems (MEMS), enabled by the very microfabrication technology for building integrated circuits, play an integral part in many of the sensors as well as in actuators (e.g., inkjet printer nozzles). The objective of this breakout session was to discuss needs, challenges, and opportunities in advancing the sensors/MEMS technologies. Seven speakers (faculty from various UC campuses and researchers from LLNL) and an additional ~15 virtual attendees participated in the session. The short presentation topics converged on biomedical and agricultural sensors, including neural interfaces, cochlear implants, optical microelectrode arrays, and radar-based plan hydration sensors. Some talks described novel fabrication methods to integrate new materials into devices. The session concluded with a lively discussion, where the key points are outlined below:

- Talks by Dr. Albert Pisano (UCSD) and Dr. Jack Kotovsky (LLNL) preceding this breakout session had offered a broad interpretation of the CHIPS and Science Act scope to include devices manufactured with materials other than just silicon and applications other than just microelectronics. Many attendees in the breakout session echoed this view and voiced the importance of sensors and MEMS and a related concern that **the CHIPS and Science Act might be inaccurately perceived to solely focus on microelectronics**. The session participants emphasized that the Sensors & MEMS should be included as a theme in the upcoming Lab Fees Research Program opportunity.
- Sensors and MEMS-based devices often use and need novel materials (e.g., nanostructured coatings) that are not readily compatible with conventional microfabrication process flow. This challenge is further compounded for devices that involve biological components (e.g., biomolecules, cells). The session agreed that **there is a pressing need for novel fabrication and packaging approaches that allow for incorporating functional materials and biochemical/biological components into the devices.**
- Signal processing, power management, and information transfer are all essential for the operation of sensors and MEMS-based devices. Often the design of these individual stages is disconnected from each other, which limits the performance of final systems due to sub-optimal power management or signal processing. The session echoed the importance of "**co-design" in researchers collaborating to design sensors/MEMS with intentional iteration between design stages.**
- While devices are routinely innovated at UC campuses and the National Laboratories, they are often manufactured in quantities that range in 1s to 10s. A challenge is mid-scale production of such devices in the order of 100s to 1000s – often necessary for pre-market studies (e.g.,

clinical trials for a new medical sensor). The session participants emphasized the need for such **mid-scale production QA/QC measures are needed. This should be coupled with versatile techniques to manufacture novel devices and later translation to partners to take on larger-scale manufacturing.**

Electronics and Photonics for Extreme Environments

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Saif Islam, Professor, Electrical and Computer Engineering, UC Davis

The field of *Electronics and Photonics for Extreme Environments* is crucial for the safety and performance of key industries, including sectors like power and energy distribution (smart grids), gas, oil, and geothermal energy exploration, tough industrial processes, transport on land, in air, space, and deep space, as well as nuclear power plants. Developing technology in these areas will create advanced electronic and optoelectronic systems that can work for many years in very hot or cold conditions, under high pressure, in chemically damaging environments, under strong magnetic fields, big shock, vibrations, and exposed to intense radiation. Essential parts of this technology are sensors that can work in these harsh conditions and co-located electronics that can process data and communicate even in extreme environments.

To address several significant engineering challenges, research and workforce training are needed in three key areas:

- Innovation materials that can work under extreme conditions,
- devices (transistors, switches, memory, sensors, etc.) and passive components that can operate reliably in these extreme environments, and
- systems that perform better than current Si-based systems and can last for decades under these extreme conditions.

The meeting included presentations and discussions on various aspects of the topic:

- High-priority challenges were recognized in nitrides, carbides, metals, oxides, borides, silicides, magnetic, insulating, refractory and ceramics materials.
- There's a need for devices capable of handling high current (e.g., 20A), extreme voltage, radiation-hardened sensing, and dealing with high nuclear radiation and nuclear waste.
- Devices that work with charged particles are particularly effective in extreme environments. Mechanical switches such as rad-hard MEMS (Micro-Electro-Mechanical Systems) were discussed as potential solutions.
- There's interest in developing technologies like terahertz (THz), photonics, plasmonics, and nanophotonic materials-based systems for potential applications in energy conversion, sensing, hyperspectral imaging, and communication under extreme conditions.

Top challenges identified by the panel:

- Material growth, doping, defects, alloy formation, reliable contacts, optical transparency, etc.
- To (in-situ) characterize materials, devices, and systems under various extreme conditions.
- Understanding and innovation in material interfaces

- The interface between the device and the system is a bottleneck. Co-located devices, sensors, and electronics are desirable (advanced packaging for extreme conditions).
- Use data science to interpret the existing dataset related to materials, defects, and reliability and use that to expedite the discovery of new materials.

Packaging, Heterogeneous Integration and Design-for-Reliability

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Albert Wang, Professor, Electrical and Computer Engineering, University of California-Riverside

Microelectronics including semiconductors and integrated circuits (IC) is the foundation of modern society, offering enabling technologies and products to support the U.S. economy and facilitate national prosperity. Historically, R&D efforts to advance information and communications technologies (ICT) have been computing-driven. As the Moore's law ends and the society fast advances into the data-driven internet of everything (IoET) era, enabling technologies are desired to tackle the complex human-world interfacing complexity, which not only requires more advanced IC chips (predominantly in Si CMOS) with higher performance, but also demands for various non-IC devices offering diverse functionalities to be hetero-integrated into Si CMOS platforms. Hence, heterogeneous integration (HI) emerges as a key technology that allows monolithic integration of different devices in dissimilar materials built in different technologies delivering the best functionalities in their native devices with advanced Si IC chips. The highly desired superior microsystem performance can only be achieved by HI technologies to deliver chip-grade system performance. As such, advanced packaging technologies are critical to achieving the highest microsystem performance, e.g., removing the die-to-die linkage barriers, enabled by HI. Furthermore, performance and reliability are the two core attributes of any IC chips and microelectronics system products. While HI allows integration of heterogeneous devices (i.e., chiplets or dielets) into Si ICs to deliver systems-on-integrated-chiplets (SoIC) of superior system performance, advanced design-for-reliability solutions are required to ensure full performance of any HI-based microsystems. Therefore, design-for-reliability emerges as the main roadblock in the heterogeneous integration roadmap (HIR).

Recommended research priorities:

- **Heterogeneous integration**: high-power devices and systems; low-energy computing devices; bio-medical devices; energy-harvesting devices; neuromorphic devices; in-memory computing devices; photonic devices; sensors; actuation devices; MEMS/NEMS; high-performance logic and memory monolithic chips, CMOS+X design methodologies, fabrication and characterization capabilities
- **Packaging**: IC-grade packaging integrating heterogeneous devices onto monolithic wafer/substrate (not traditional printed circuit boards or system-in-packaging formats); neighboring interactions in packaged SoIC microsystems; new packaging materials; leveraging IC fabrication technologies and infrastructure for advanced packaging at wafer/substrate level.
- **Design-for-Reliability:** Electrostatic discharge (ESD); self-heating effect (SHE)-induced overheating, in-die temperature sensing, full-chip thermal mapping with transistor-level

resolution, dynamic thermal management; cooling; radiation harness; mechanical failures; failure tolerance and resilience.

The session participants identified the following specific challenges:

- Inter-chiplets interconnects,
- Advanced ESD protection concepts, design methodologies, designs and characterization
- ESD-RFIC co-design for next-G RF ICs.
- ESD-technology co-development for advanced IC technologies
- Novel in-die thermal sensing technology enabling full-chip thermal mapping with transistor-level spatial resolution
- full-chip true dynamic thermal management for SoCs and SoICs
- Co-design, co-development, co-optimization (from atoms to architectures: materials, technologies, devices, circuits, systems)
- The importance of continued research in logic transistors and memory for heterogeneous integration of high-performance monolithic chips.
- Prototyping by hetero-integrating different materials and devices into microsystem chips to achieve ultimate system chip performance
- Mid-volume fabrication of heterogeneous SoIC chips
- Modeling and EDA tools supporting SoIC designs
- Across-boundary (materials, chiplets, full-packaging) modeling and simulation
- Characterization of HI SoIC chips
- Recycling high-volume materials
- Low-environment-impact fabrication processes

Modeling and Simulation for Microelectronics

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Roger Lake, Professor, Electrical and Computer Engineering, UC Riverside
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Modeling and simulation plays an important role in the R&D of microelectronic devices as it provides a “virtual prototyping” facility to evaluate many different design options before the costly process of actually synthesizing the materials or building the devices has commenced. In so doing, a very broad design space of potential realizations of an advanced microelectronics device or material, or architecture can be evaluated for its performance potential before it is ever built. Figure 1 shows a vision of a full atoms-to-architectures “virtual prototyping” capability that enables modeling of

microelectronics systems from the performance of bulk materials, to devices, to entire system architectures that deliver performance benefits for the target applications.

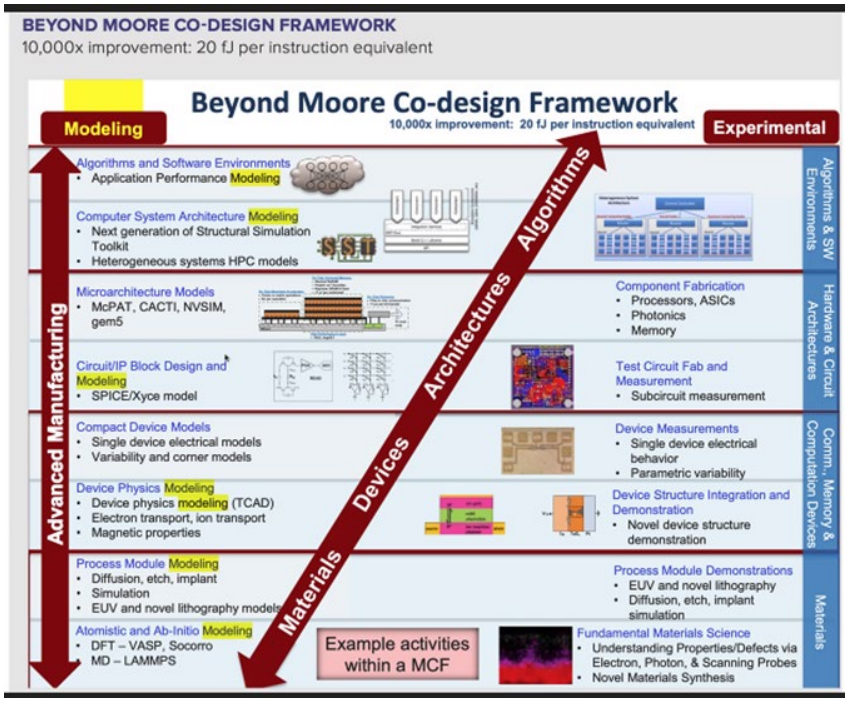

Figure 1: Modeling of microelectronics from materials to architectures to accelerate translation of technology from lab to fab. From the Report of the Office of Science Workshop on Basic Research Needs for Microelectronics, 10/2018, p. 68. Original courtesy Matt Marinella, Sandia.

Challenges: Bridging between the layers and length-scales is the toughest part (so hard that researchers typically don't do it). Scientists can make entire careers working at one layer, but working on one layer doesn't advance the translation of the technology to realizable solutions unless all layers can be spanned. The development of this kind of cross-layer modeling capability is not strictly technological. There are social aspects as well. We need to build trust, and the skill and vocabulary to communicate between the layers. Figure 1 expresses a vision for breaking through those layers and developing a framework for codesign of microelectronics that integrates efforts all the way from fundamental material science all the way up to full architectures and applications.

Solutions: LFRP should encourage exchanges where universities operating at layer A send students to embed with a lab research group at the next layer up (and vice versa).
We can build on top of ECP-developed frameworks such as AMReX, ARTEMIS, FerroX, and WarpX, so we are not always starting from scratch.

Discussion on Modeling and Simulation Codes

In microelectronics, current low-level modeling efforts transition from density functional theory calculations of bulk and thin-film material and heterostructure properties to atomistic and discretized continuum models of devices. This dual approach is driving the development of next-generation electronic devices and materials, from ultra-low-voltage electronics to superconductors. Programs like exascale code packages utilize massively parallel systems to understand microscale physics, while computational methods identify materials with desired properties, enhancing device performance and efficiency. Modeling efforts extend to electronic, spintronic, phononic, magnetic, and magnonic properties of low-dimensional materials, addressing challenges like heat dissipation, phonon transport, magnon and spin transport, and the effects of confinement and high electric fields. This comprehensive

approach, combining advances in fundamental materials science with device engineering solutions, is crucial for overcoming current limitations and paving the way for future microelectronics, emphasizing economic viability, environmental sustainability, and security.

The development of architecture simulators, such as the next-gen gem5, supports the transition from logic blocks to systems, incorporating new computing architectures and emerging workloads. This journey from device-scale simulations to system-level models involves multiple fidelity levels, from detailed device modeling to circuit and system-level simulations using AI/ML-powered Electronic Design Automation (EDA) tools. EDA is crucial for scaling up microelectronic designs efficiently, requiring precise models for success. The construction of these models enables EDA tools to accurately predict performance for informed engineering decisions. Addressing the challenges in this field could benefit significantly from research funding, potentially turning obstacles into collaboration opportunities between universities and labs. Several issues have been identified, such as the need for open-source Process Design Kits (PDKs) to bypass legal constraints, the challenge of scaling across different dimensions of modeling, and the discrepancy between models and actual circuits. These problems highlight a broader issue of communication and trust across different levels of simulation and design.

The challenges in creating a comprehensive digital twin, through a co-design approach that spans multiple institutional layers, are complicated by career specializations at specific length scales and the difficulty of communication across these layers, making it hard to bridge gaps essential for a fully integrated model. There is a consensus on the need for a collaborative approach to bridge these gaps, involving both educational initiatives and technological advancements. Suggestions include developing AI-enabled simulation approaches, leveraging High-Performance Computing (HPC) for PDE solutions, and creating more computational frameworks. An integrated educational program, involving guest lectures from lab staff and real-world projects, could enhance workforce development. Additionally, facilitating access to user facilities and exploring in-kind funding are essential steps toward achieving these goals. Addressing these needs requires a concerted effort to enhance microelectronics modeling and simulation capabilities, underscoring the importance of collaboration between academic institutions and National Laboratories.

Discussion of Access to HPC Facilities

Challenges: Modeling and simulation of microelectronics materials, devices, and systems is resource intensive and requires access to HPC resources. UC researchers need reliable and scalable access to HPC resources to make productive use of the modeling capabilities envisioned in the prior section

Solutions: There are numerous HPC facilities distributed across the University of California system.

- Access to NERSC at LBNL
- Access to ElCap at LLNL
- Access to UCSD NSF Supercomputing Center
- Access to intensive training to be able to use these resources
- Access to HPC at UCL

As part of this LFRP project, the UC could create a coordinated pooling of discretionary cycles for these resources across the UC System. This would ensure reliable access to these resources to ensure the success of LFRP funded projects.

Discussion of Access to Laboratory National User facilities

Challenges: Many of the resources for prototyping, metrology, and in general simulation/modeling are distributed across the UC. Many of these resources are unique and not replicated at other campuses.
Solutions: The national user facilities have mechanisms to provide access to these capabilities and need to find a way to normalize the availability and access across the UCs.

Discussion of Workforce Development
Challenges: Few UC's offer classes on modeling and simulation, much less for microelectronics
Solutions: Lecture series or even distance learning class team taught by lab researchers and UC faculty (rotate through diverse speakers to cover different topics); teach through zoom to all campuses potentially recorded for posterity; have microelectronics focused capstone topics for UC students that are aligned with targeted microelectronics topics.

Quantum Devices

Kristin Beck, Director, Livermore Center for Quantum Science, Lawrence Livermore National Laboratory
Shane Cybart, Professor, Electrical and Computer Engineering, University of California-Riverside

Quantum devices include and represent a broad range of novel physical hardware systems that will enable computations that are currently impossible. While there are many important and large challenges on the horizon for these developing technologies, four themes emerged from contributed presentations from the National Laboratories and University of California campuses:

- Connecting the quantum and classical worlds,
- Novel approaches to highly coherent qubits,
- Leveraging quantum devices for ultra-low-power classical computing, and
- Fostering workforce training in quantum devices and cryogenic system engineering.

Connecting the quantum and classical worlds. For quantum computers to become useful, large quantum systems will need to be controlled from room temperature and return results to that less controlled environment. For superconducting systems, simply scaling current approaches would introduce too much hardware and heat load into cryostats. New engineering approaches are needed to overcome this anticipated bottleneck, such as developing cryogenic digital controls that operate at temperatures less than 4K. Viable technologies involve integration of qubits with cryo-CMOS, superconducting single flux quantum (SFQ) logic and quantum flux parametron logic. Other approaches involve transporting quantum control signals on optical carriers over fiber instead of on metal wires and developing low-mass (and low-field) quantum amplifiers and isolators that operate at the quantum limit. A technically simpler, yet no less important problem, is the classical control stack for quantum computing. Commercial systems are expensive, yet they don't perform. Application specific controllers may need to be developed for quantum control that balance research flexibility with timing and fidelity considerations to enable research systems to test larger systems.

Novel approaches to highly coherent qubits. For a quantum system to be used for computation or sensing, the quantum system's phase and energy must be unperturbed by its environment. This coherence time is a typical timescale for the system to perform as a quantum one. Highly coherent devices will enable useful quantum applications. The root causes of decoherence need

to be better understood and linked to material properties. Historically, improved fabrication, materials control and engineering design improvements have enabled coherence times to improve on the frontrunner qubit modalities. These approaches reduced two-level systems in surface oxides and engineered phonon band-gaps to isolate superconducting qubits from their phonon environment. For ion trap qubits, 3D printing has been used to generate deeper potentials that are less sensitive to electric field noise. More improvements and innovations in existing approaches are needed, as well as new qubit modalities.

Leveraging quantum devices for ultra-low-power classical computing. Adiabatic quantum flux parametron (AQFP) logic and some superconducting microwave qubits that switch with just a single microwave photon of energy are extremely efficient logic devices. AQFP circuits operate with an average bit energy six orders of magnitude lower than CMOS. These devices enable ultra-low-power digital classical computing and high-performance, neuromorphic and reversible computing. Reversible computing operates at energies below the fundamental Landauer limit from thermodynamic information theory. The Landauer limit at 4.2K is an energy level of 4.019e-23 J that is derived from the fundamental entropy of two logic states S =kB ln 2. In reversible computing, entropy does not increase because the logic is symmetric, meaning that the answer can be fed backward through the circuit to generate the question. This removes the limit on the dissipation energy. Before the development of AQFP, the field of reversible computing was predominately a theoretical one with experimental demonstrations limited to processes in biological molecules and quantum dots. Now, however, it is possible to build and test experimental AQFP gates that operate at the lowest energies of any logic device.

Memories. An important active research area related to both qubits and superconductor digital logic is integration with a high-density cryogenic memory. Possibilities include cryogenic compatible CMOS devices that can operate at the ultra-low temperatures required for quantum circuits and novel forms of superconducting digital logic memories. Reduction in power consumption is an important area for cryo-CMOS, while scalability down to smaller sizes is the top research priority for superconducting memories.

Workforce Development. There is a critical need for workforce development and training in quantum electronics, especially in engineering. Quantum electronics require much greater care in mitigation of electromagnetic interference, and precision measurement of signals from Josephson junctions that are a million times smaller than CMOS. It also requires expertise in cryogenic cooling and vacuum systems. Many of the careers in quantum electronics require US based persons capable of obtaining security clearances. There is a shortage of doctorate level human resources in this important area in the National Labs and industry.

NextGen Electronics Materials and Devices

Yu-Hwa Lo, Professor, Electrical and Computer Engineering, UC San Diego
Peter Fischer, Senior Scientist, Materials Sciences Division, Lawrence Berkeley National Laboratory and Adjunct Professor in Physics, UC Santa Cruz

Future microelectronics will rely heavily on our ability to explore new approaches, e.g. exploiting topological spin textures (Skyrmions, Hopfions, etc.), to further miniaturize components and to move information between different parts of a computer chip at high speed, and most importantly requiring

orders of magnitude lower power than what is available today. An accelerated discovery and development of the next generation of electronics materials and devices is of paramount importance, but we need to also recognize economic viability, environmental sustainability and national security aspects. A co-design approach combining advances in fundamental materials sciences which are intimately connected to engineering solutions up to the system level is most promising and bodes well by leveraging the individual strengths at UC campuses with the unique capabilities at National Laboratories.

Basic materials science efforts will not only aim to predict, understand, and control properties and behavior of next generation electronic materials across several length and time scales, but will focus on investigations of materials interfaces since “the interface is still the device” and a deeper understanding of how materials interact with each other will discover new physics and will lead to transformative technologies.

Novel methodologies and advanced capabilities, e.g. future scalable metrologies will leverage advances in computational and modeling tools, so that not only novel materials can be predicted, but assembled into entire functional electronic devices. Integration of AI/ML in all aspects of the scientific and technological efforts towards next generation materials and devices will be a key for acceleration. Specific examples are the Integration of state-of-the-art theory, calculations and materials informatics, e.g. in the Materials Project at LBNL, a co-design concept, e.g. in AI-automated microelectronics research that incorporates theory at several levels of the discovery process connected with an AI/ML driven feedback circle between advanced synthesis and characterization techniques, such as x-ray and electron based spectromicroscopy and scattering at DOE user facilities, and simultaneous efforts in device design using Exascale modeling towards real device fabrication.

To expand this basic research towards a higher TRL level, one needs to address essential technology challenges, e.g. advanced lithography and high precision patterning, where again the interface challenges mentioned above will be dominant. A widely discussed class of potential future electronics materials are 2D materials. To achieve low-power electronic devices, the implementation of voltage control to switch magnetic moments is a promising direction.

Enormous opportunities for collaborative R&D between UCs and National Laboratories could be in novel non-van-Neumann computing architectures. An example is neuromorphic computing, e.g. with memristive systems or Josephson junctions, for the development of basic functionalities, e.g. the design of electronic neurons and synapses Neuromorphic computing is modeled after the human brain. It is not digital logic in the style of current computers but relies on probabilistic conclusions based on a long-range interacting set of coupled devices. A novel demonstration from UCSD has shown neuromorphic logic utilizing disordered superconducting loops coupled by Josephson junctions. In addition to showing high frequency performance, it has demonstrated associative learning behavior which traditional semiconductors do not. Furthermore, it consumes 10**6 less energy than Moore's Law machines.

Other concepts for advanced manufacturing could include magneto-dielectric composites.

The human capital at both the UC campuses and the National Laboratories is probably the most important asset when establishing successful collaboration as part of the endeavor to develop the next generation of electronics materials and devices. A highly transparent and fluid exchange of students, postdocs, researchers, engineers, and technicians between the various collaborating institutions needs to be established.

When defining collaborative scientific projects, a thorough assessment of the scientific alignment will be key for success. This will entail the implementation of compatible experimental, modeling and data platforms for a rapid adjustment and distribution of tasks among the partners. It will train an agile and creative future workforce which will be essential to meet the challenges of future microelectronics as probably the most relevant key technology.

Wireless Technologies

Peter Asbeck, Professor Emeritus, Center for Wireless Communications, CALIT2, UC San Diego
Danijela Cabric, Professor, Electrical and Computer Engineering, UC Los Angeles

The area of Wireless is broad and covers not only RF electronics to implement connectivity but also modulation protocols, networking and security, sensor development and applications. Accordingly, there were presentations and discussions on a variety of topics, briefly summarized as follows:

- Ian Galton (UCSD) discussed high sampling rate analog-to-digital converter development implemented with scaled Si CMOS, which is primarily oriented towards digital electronics.
- Gabriel Rebeiz (UCSD) covered work on phased arrays and RFIC design, including development of 5G/6G and related phased-arrays for joint communication and sensing.
- Albert Wang (UCR) discussed technology to convert existing LED lighting infrastructure into optical wireless networks, and related future needs for heterogeneous integration with CMOS.
- Patrick Mercier (UCSD) presented techniques for RFID-like battery-free operation using a single mobile phone and opportunities for wearable sensors and bio-energy harvesting.
- Dinesh Bharadia (UCSD) discussed multimodal wireless localization techniques for mobile computing platforms and autonomous robots trained with deep learning to provide contextual information and navigational directions.
- Shaya Fainman (UCSD) discussed novel photonics novel technology and possible uses for routing on-chip and between chiplets.
- Hanh-Phuc Le (UCSD) discussed integrated power electronics and energy-efficient systems including signal-dependent power-tracking for efficient RF systems.
- Danijela Cabric (UCLA) discussed issues for cognitive radio, whereby temporarily unused portions of the rf spectrum can be identified and shared by potential users.
- Ryan Goldhanh (LLNL) presented goals for National Labs including systems under strict size, weight, and power constraints; proliferation of small (and increasingly multi-modal) sensors; performance in low SNR, high interference regimes, and integrated sensing and communication.
- Peter Asbeck (UCSD) summarized projects within the UCSD Center for Wireless Communications, led by Sujit Dey, including AI-6G; circuits for 5G/6G, connected health, connected and autonomous vehicles, wireless AR/VR, and RF Safety.

Critical technical challenges facing the wireless area and possible methods of addressing them were discussed. Growth rate of wireless data rate over the past 25 years has been more rapid than Moore's Law; the number of global mobile subscribers now exceeds the population of the planet; a new wave of explosive growth is imminent, with the Internet of Things. Key challenges include 1) finite RF spectrum 2) finite power per user 3) interference and security problems; 4) development for specific application issues.

Topics which strongly overlap with National Lab interests include:

- Heterointegration and advanced packaging to enable high performance electronics in small footprints with improved heatsinking
- Advances in microelectronics towards higher frequency operation, not just for digital circuits, but also for RF, for power converters, and very importantly, for mixed signal circuits (analog-to-digital and digital to analog converters)
- High frequency device and circuit characterization and measurement techniques
- Modeling and simulation of complex 3D systems including mechanical, thermal and electrical characterization
- Ultra low power sensors to connect to the world at large, enabling Internet of Things with minimal battery requirements
- Biomedical and wearable electronics
- Applications of wireless technology together with AI to address needs in health, transportation and education
- Digital predistortion and correction of signals

Also discussed was a topic not currently addressed: the need to better understand the ethical, legal and social implications of providing AI to every person around the globe.

Electronic Design Automation (EDA)

Sheldon Tan, Professor, Electrical and Computer Engineering, University of California-Riverside

EDA solutions are essential in chip manufacturing despite not directly manufacturing chips. EDA provides several crucial functions. First, in Technology Computer-Aided Design (TCAD), they aid in designing and validating devices and semiconductor manufacturing processes for optimal performance and density. Second, they provide the synthesis flow from high level design concepts like algorithms to physical layouts suitable for manufactures. Furthermore, in Design for Manufacturability (DFM), they optimize layouts and verify designs to ensure they meet manufacturing requirements, mitigating functionality and reliability risks. Third, they simulate and verify the designs via sign-off process to ensure successful silicon chip fabrication for targeted foundry. Fourth, in Silicon Lifecycle Management (SLM), they monitor chip performance post-manufacture to deployment, aiming to maintain expected performance and prevent tampering.

Dr. Dilip Vasudevan of LBNL commenced the session with a presentation on the "Beyond Moore's Law Computing Project" at the Computer Architecture Lab, followed by flash presentations by Dr. Zheng Zhang and Dr. Sheldon Tan to introduce some of the research works for potential collaborations. The discussions revolved around potential research collaboration avenues and workforce development (WFD) requirements across UC National Laboratories.

Emphasis was first placed on fostering a skilled workforce from universities to contribute to the development of EDA tools, spanning traditional CMOS flow using open-source platforms like OpenROAD and extending to merging beyond-Moore devices. The roadmap from LBNL's PARADISE

to PARADISE++ and research into beyond-Moore law (BML) microelectronics offered promising collaborative opportunities for co-design flow development, bridging between different layers of PARADISE/PARADISE+ framework, device simulation and modeling of novel BML devices like MESO, NCFET, skyrmions, RSFQ, and MRAM/RRAM. The applications for the proposed beyond Moore's law computing includes climate modeling, density functional theory (DFT), genome sequencing, and generative AI acceleration.

There is a pressing demand for **open-source EDA tools** like OpenROAD, given the limited accessibility of commercial alternatives in UC labs. Efforts to enhance the involvement of labs with the research and developer/user community in deploying OpenROAD and other open-source EDA tools are needed. Moreover, there is a need for tools and workflows to support enablement tasks such as PDK development for new BML devices and MRAM/RRAM devices. For instance, the potential of OpenDRAM at U. Kentucky could address this need. Additionally, there is a necessity for AI enabled assistants or agents like the recent NVIDIA ChipNeMo chatbot for EDA design flow to reduce the learning and training curves for using the open source and commercial EDA tools.

There are also strong needs for **efficient and fast technology CAD (TCAD)** and device modeling capabilities for new devices where recently proposed scientific machine learning methods should be investigated. EDA design flow for photonics for both interconnect and computing are also needed. Strategies for open-sourcing planning and promotions within UC and UC National Labs are also imperative to foster collaboration and innovation in semiconductor research.

Proposed collaborative projects also include **ML/AI enabled fast simulation and compact modeling** using physics-informed neural networks (PINN) at various levels (from devices/TCAD, circuits and system levels) and automation for optimal processes to calibrate reduced/compact models. EDA-inspired AI (sustainable training on cloud and edge, self-healing trustworthy AI systems), efficient tensor compression for AI training, thermal visualization and modeling of hot spots and power of commercial and new BML chips and processors and emerging AI accelerators chips like GPUs and TPUs.

Partnerships and Training Opportunities *[~ 2 pages]*

The conversation around workforce development and training centered on how long-term relationships between individual UC PIs, students, and National Laboratory researchers both strengthen the connections between the UCs and National Laboratories and create meaningful learning experiences that come with deep interpersonal networks within the national laboratory for the students.

Workforce Training in Microelectronics in the USA

There is a recognized shortage of skilled workers in the field of microelectronics in the USA, driven by advancements in technology, expanding applications, geopolitical factors, and the retirement of experienced professionals. This shortage has notably impacted the design and manufacturing industry, research institutions, and university students. A significant effort is underway within Federal agencies and the microelectronics industry to tackle this urgent issue. Initiatives like CHIPS and the Science Act are pivotal by facilitating cutting-edge research and manufacturing facilities, boosting

resources to improve workforce training, and fostering innovation in microelectronics. All levels of the microelectronics supply chain need to be addressed from device modeling, design, fabrication, materials characterization, electrical testing and system integration. Collaborations with National Laboratories through LFRP projects present opportunities for expediting progress and achieving impactful outcomes.

Based on the suggestions and comments of the labs and UC participants, here are some areas where UC Laboratories and the UC campus can collaborate to address the workforce shortage and strengthen partnerships:

- **Student Training:** UC-affiliated National Laboratories are rich in resources for design, manufacturing, testing, and prototyping. These can help effectively train undergraduate and graduate students through increased involvement in internships, extended lab stays, mentorship, and collaborative thesis research projects. There is a potential for accommodating more users in the materials, fabrication, and characterization facilities in the UC Laboratories. In future workshops, students at different career stages should be included to obtain their perspective on what training opportunities could be most valuable/effective for them. In addition to longer term internships, there are opportunities to develop programs modeled after the LLNL/Data Science Challenge where students from a wide range of educational backgrounds are introduced to the field with a 2-week program that incorporates a mini project, which sets them up to be competitive for internships in future years. Utilizing National Laboratory resources such as the LLNL and LBNL quantum testbeds in long-term collaborative thesis work for UC students, and working with the National Laboratories to have flexible student terms that support continued work on mutual projects, more akin to a visiting researcher appointment than to summer internships.
- **A consolidated list of lab/fab resources**: A list of equipment in National Laboratories and UC Campus-based shared labs/fabs can help create adequate redundancy for shorter downtime and higher efficiency. A mechanism of efficient communication between facility directors, such as email distribution lists or platforms such as Slack or MS Teams.
- **Technician Training/Reskilling Programs:** In California Community Colleges, approximately 60% to 65% of students conclude their educational journey at the community college level, with only a small number transferring to institutions such as UC campuses. Training technicians and reskilling the workforce from other related sectors or outdated technologies can benefit the microelectronics industry ecosystem. Leveraging the extensive state-of-the-art facilities and resources of UC Laboratories can play a significant role in providing this training. An alliance of industry associations, community colleges, UC campuses, and UC Laboratories can play active roles.
- **Engagement of Students and Teachers of K-12 Entities**: Introducing microelectronics at the K-12 level is crucial to building a strong interest in the college levels and raising awareness about microelectronics career opportunities. This involves hands-on workshops for students, teachers at the university, National Laboratories, and K-12 campuses to expose students to exciting career opportunities in the field and partnerships with community organizations, particularly those working with underrepresented groups. Integrating experiential learning into the classroom environment that enables students to learn more about topics of current interest and could feed into national laboratory internship programs.

- **Shared appointments, sabbaticals and faculty exchanges:** Initiatives like the ***de minimis* teaching agreement** collaboration between UC Berkeley and National Laboratories can be used as blueprint for other UCs. This agreement allows researchers from National Laboratories to teach one course every two years at UC Berkeley, encouraging interaction with students and inspiring them for internships and future positions. Dual and joint appointments, where individuals split their time between the lab and campus, further strengthen collaboration by enabling direct access to students and promoting research partnerships. These collaborative efforts have been successful and hold potential for further expansion, benefiting both participating institutions.

Partnering with the National Laboratories

Los Alamos National Laboratory offers numerous opportunities and mechanisms that foster university engagement and R&D partnerships. In addition to encouraging informal intellectual commerce, LANL, under the management of Triad, LLC, has established the **LANL Partnerships and Pipeline Office (PPO)**, which offers formal programs and mechanisms that enhance connections to universities and their faculty members. The PPO comprises centers and program offices that are coordinating entities for university engagement, R&D collaborations, recruiting, and workforce development. The University Collaborations Office within NSEC is a resource that can help to forge connections between interested UC faculty and LANL researchers should the proposed research fall outside the purview of the Institute of Materials Science (IMS) or the Information Science and Technology Institute (ISTI). Dr. Heather Erpenbeck (hawk14@lanl.gov) is the current leader of the University Collaborations Office.

The recent workshop was focused on the lifecycle of microelectronics research and development and brought together a diverse community of researchers in, among many areas of interest: novel and next-generation materials discovery; quantum devices and computing; design automation; device design, packaging, and integration; and device/system performance in real environments. These areas of cutting-edge research align with the interests and charters of two NSEC institutes: the IMS and the ISTI. Interested UC faculty can engage with LANL researchers in a meaningful way by connecting to the Laboratory through these institutes.

The Academic Engagement Office (AEO) at **Lawrence Livermore National Laboratory** was established to foster collaborations and sustain long-term academic partnerships between Laboratory researchers and academic institutions. The AEO hosts a wide variety of programs that engage students and faculty in collaborative research and development, work study opportunities, and educational activities that support the Laboratory's programmatic objectives, address national security workforce needs, and enhance community awareness and understanding of science. Dr. Eric Schwegler (schwegler1@llnl.gov) is the current Director of the Academic Engagement Office.

The **Lawrence Berkeley National Laboratory** continually looks for ways to both expand existing collaborative efforts with its UC colleagues as well as explore opportunities to bring the Lab and broader UC expertise together to discover new approaches to difficult research questions. As a fully UC-managed lab, LBNL benefits from this unique relationship, and their Research Areas have close

collaborations and joint relationships that support the development of these partnerships. LBNL seeks to engage UC researchers and their teams directly with their Research Areas, or through other programs such as those within the Workforce Development and Education Office, its home for various DOE supported internships for undergraduates, graduate students, and faculty. Those interested in learning more about engaging with LBNL are welcome to reach out to Bill Johansen, Senior Advisor to the Deputy Lab Director for Research (wejohansen@lbl.gov).

Another unique resource for UC researchers is access to the **UC Livermore Collaboration Center (UCLCC)**. The UCLCC is a system-wide UC asset that offers a robust collection of capabilities and facilities aimed at connecting people and ideas across UC's campuses, medical center, and UC-affiliated National Laboratories. Anyone affiliated with UC is welcome to request use of the space for any challenge that demands diverse expertise, but UCLCC's primary focus is hosting creative programs in three anchor areas: high energy density science, materials and manufacturing, and data science and artificial intelligence. UCLCC was a key collaborator and host in the development of the LFRP workshops.

In conclusion, the two LFRP workshops are particularly useful examples of venues to connect UC faculty with researchers and administration of UC labs to establish potential collaborations. Additional workshops should be conducted with a different focus before the LFRP calls in the future. A mechanism to support UC and National Laboratory workshops outside the LFRP cycle would also be of great benefit. More graduate students, especially underrepresented and female students, should be encouraged to participate in such workshops in the future. Perhaps providing an opportunity for a student-centered session or parallel activity during the workshop.

Sustaining and Extending Partnerships beyond the Workshop

A common challenge with workshops is sustaining the momentum and reducing the discussions into a well-defined proposal/project. Several potential mechanisms and ideas to sustain activity beyond the workshop were discussed during the plenary sessions and breakout groups at the workshops:

- **Finding collaborators and partners**: A portion of the discussion revolved around the barrier that exists for individual professors (especially early career professors) to get enough visibility into the National Laboratories to start new collaborations. This included developing enough knowledge of the capabilities, research thrusts, and individual contributing scientists to have a connection point. Even for more senior staff, a theme of the conversation was that the UC/National Laboratory community could do more with existing resources given better connections between researchers and specific fabrication and/or characterization facilities such as deposition systems, cryostats, single photon sources, and high-resolution spectroscopes. UC researchers were invited to contact the National Laboratory Academic Partnership leads, or use the resources provided by the UCLCC team to aid in making connections.
- **Conferences, workshops, and seminars:** Programs that bring lab scientists to the UC campuses for seminars, lectures and research would help with greater student contact and

more interaction. The UC-affiliated National Laboratories have established programs to support faculty sabbatical appointments at the labs, as well as Professional Research or Teaching (PRT) opportunities for lab staff. These programs present a great opportunity not only to enhance the mutual understanding of resources and capabilities between the institutions but also to cultivate meaningful collaborations and enduring partnerships between the National Laboratories and the UC campuses.

- **Student and postdoc engagement:** Creating and publicizing opportunities for student internships and fellowships, targeted summer schools, Postdoctoral appointments, and fellowships.
- **Seed funding programs:** To nurture future collaborations, participants suggested providing seed grants for faculty and students from universities to visit a specific National Laboratory for a few days to network with staff in their area and to get to know the National Laboratory's capabilities. A good example of a successful seed funding program is the **MICRO+ Funding Program.** Some attendees felt the prior UC MICRO Funding Program was a success and that at this critical time, UCOP, in collaboration with CA industry should consider launching a new MICRO+ Funding Program. Small seed funding awards to kick start new research collaborations would also be of strategic value.
- **Communication platforms:** Leveraging communication platforms to share information about engagement opportunities, events, funding opportunities, and connections. Several researchers shared their positive experiences using platforms such as Slack or Teams, and using email lists, webpages, and newsletters to disseminate information.
- **Sustainability:** assisting teams in identifying extramural funding, supporting the development of joint proposals to sponsors, creating curated funding searchers, and teaming support.
- **Research development staff**: The upcoming Lab Fees Research Program funding is certainly a valuable opportunity to bring researchers across the UC campuses and the National Laboratories together. However, this can be prohibitive for some projects where researchers do not have the required collaborations across different campuses and National Laboratories to be able to submit such a proposal. In general, a champion for a topic is required to pull together a competitive proposal and manage the project if funded. These pursuits require significant faculty and staff time. Additional staff support (even to help the faculty stay on track with well-defined timelines) may increase the probability of sustaining the exciting ideas that emerge from the workshop.
- **Access to user facilities:** raising awareness of programs and mechanisms to access both UC and National Lab user and shared-use facilities. The proposal to create a directory of relevant facilities across the UC system and National Labs was unanimously supported by the workshop participants.
- **Partnership with other national workforce development (WFD) programs:** For example, the American Semiconductor Academy (ASA) Initiative and the ASA-SEMI Partnership that aim to establish a national microelectronics education and training network (involving ~60 universities, ~60 community colleges and ~45 company endorsers). The proposed **California Microelectronics Institute** was cited by some participants as an exemplar microelectronics education and training infrastructure to address the national semiconductor WFD problem. CSI could partner with the industry (SEMI, companies in Silicon Valley) closely for WFD to make national impacts. They envision that establishing CSI will give UC the advantage to ask for more

federal funding for WFD (e.g., CHIPS Cat) and attract the Center for Excellence for WFD (DoC CHIPS NSTC/NAPMP funding) to California. They remarked that other regions and university systems have been very active in this area.

Workshop Title: Research Advancing Microelectronics
Host/Coordinating Institution: UC Davis
Workshop PI Name: Davis, Cristina
Workshop Report Authors: Davis, C., Cordova, A.L., Islam, S., Seker, E. [UC Davis]; Erpebeck, H., Rondinone, A. [LANL]; Shalf, J., La Fontaine, B., Johansen, W., Yao, Z. [LBNL]; Kotovsky, J., Haque, R., Schweickert, M., Nikolic, R., Schwegler, E., Beck, K., Voss, L. [LLNL]; Cybart, S., Lake, R., Wang, A., Tan, S. [UCR]; Asbeck, P., Lo, Y., Rao, R. [UCSD]; Fischer, P. [UCSC/LBNL]; Cabric, D. [UCLA].

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Appendix: Workshop Agendas

Advancing Microelectronics Workshop #1

Date: January 19th, 2024
Location: UCLCC, Livermore, CA

8:15 am	**Lawrence Livermore National Laboratory – Facilities Tour** Host: Jack Kotovsky, Ph.D., Micro and Nano Technology Section Leader
9:00 am	**Registration and Networking Breakfast**
9:30 am	**Welcome and Opening Remarks: UC Livermore Collaboration Campus (UCLCC)** Camille Bibeau, Ph.D. Executive Director, Partnerships and Outreach UC National Laboratories University of California Office of the President
9:45 am	**The UC National Laboratory Fees Research Program (LFRP)** Rebecca Stanek-Rykoff, Ph.D. Program Officer, UC Research Initiatives & Interim Co-Associate Director, Lab Fees Research Program Research Grants Program Office University of California Office of the President
10:00 am	**Research Advancing Microelectronics: Challenges and Opportunities** Moderator: Cristina Davis, Professor and Associate Vice Chancellor for Interdisciplinary Research, UC Davis Tsu-Jae King-Liu, Professor and Roy W. Carlson Chair in Engineering; Dean of Engineering – UC Berkeley Albert Pisano, Professor and Walter J. Zable Endowed Chair of Engineering; Dean of Jacobs School of Engineering – UC San Diego Q&A
11:00 am	**Break**

	Advancing (Micro)electronics (and MEMS, packaging, sensors, materials...) Research
11:15 am	Lawrence Livermore National Laboratory – Jack Kotovsky, Ph.D., Micro and Nano Technology Section Leader Lawrence Berkeley National Laboratory – John Shalf, Ph.D., Department Head for Computer Science Los Alamos National Laboratory – Adam Rondinone, Ph.D., Co-Director for the Center for Integrated Nanotechnologies (CINT) and Group Leader for MPA-CINT Q&A and discussion
12:15 pm	**NETWORKING LUNCH**
Session I **1:45-2:45pm** **Break** **2:45-3:00pm** **Session II** **3:00-4:00pm**	**Breakout sessions** Participants will be allowed 6 min for a flash presentation following the provided template. A discussion session will follow the presentations. You can share your presentation by uploading here: Presentations. There will be a break at 2:45 pm, and participants will have the option to join a different room. **Electronics and Photonics for Extreme Conditions** Devices, sensors and systems with exceptional thermal and chemical stability, high electrical endurance (e.g., high breakdown voltage), high radiation tolerance, high oscillation frequency, and extraordinary reliability. These systems are expected to operate in harsh environments such as high temperatures, cryogenic temperatures, high pressure, high shock, extreme mechanical vibration, high radiation, erosive flow, corrosive media, electrostatic discharge, electromagnetic interference, and intense optical intensities. Moderators: Saif Islam (UC Davis) & Rebecca Nikolic (LLNL). **MEMS and Sensors** Any type of MEMS structures heterogeneously integrated with semiconductors, stand-alone MEMS. Moderators: Erkin Seker (UC Davis) & Razi Haque (LLNL) **Packaging, Heterogeneous Integration and Design-for-Reliability** Continuous advances in chips must handle merging challenges such as 3D packaging, chiplets, heterogeneous integration, thermal management, design-for-reliability, fault tolerance and resilience, etc. Moderators: Lars Voss (LLNL) & Albert Wang (UCR) **Modeling and Simulation Challenges** Materials, device and systems-scale modeling tools. Digital twins, AI, and scalable modeling techniques.

	Moderators: Roger Lake (UCR), John Shalf (LBNL) and Jackie Yao (LBNL)
	Breakout Reporting
4:00 pm	Breakout leads/moderators will provide a brief summary of main points discussed, and any point the group recommends be addressed during the next workshop.

Advancing Microelectronics Workshop #2

Date: January 30th, 2024
Location: Qualcomm Institute, CALIT2, San Diego, CA

8:30 am	**Registration and Networking Breakfast**
9:00 am	**Welcome and Opening Remarks and Workshop #1 Recap** ● **Ramesh Rao**, Professor, Electrical and Computer Engineering Director, California Institute for Telecommunications & Information Technology, Qualcomm Institute, UC San Diego ● **Albert Pisano**, Professor and Walter J. Zable Endowed Chair of Engineering Dean of Jacobs School of Engineering, UC San Diego
9:20 am	**Engaging with our National Lab Partners: Academic Partnerships and Programs** ● **Heather H. Erpenbeck**, University Collaborations Office National Security Education Center (NSEC), LANL ● **Bill Johansen**, Special Assistant to the Deputy Laboratory Director Laboratory Directorate, LBNL ● **Eric Schwegler**, Director of the Academic Engagement Office, LLNL
10:00 am	**Research Advancing Microelectronics: Challenges and Opportunities** ● Moderator: **Robert C. Dynes**, President Emeritus, University of California ● **PR Chidi Chidambaram**, Vice President of Engineering, Qualcomm Technologies ● **Yu-Hwa Lo**, Professor, Electrical and Computer Engineering; CA DREAMS Hub
11:00 am	**Break**

11:15 am	**CHIPS+S: Funding Landscape and Opportunities (30 min)** ● **Phil Harman**, Director of Research, Federal Governmental Relations. University of California Office of the President
12:00 pm	**NETWORKING LUNCH**
1:30 pm **Break** **2:45-3:00**	**Breakout sessions/Working groups** **Quantum Devices** Ultra efficiency and performance, non-classical computational approaches. Digital superconducting, interconnects between quantum and classical comp. Moderators: Shane Cybart (UCR) & Kristi Beck (LLNL) **NextGen Electronics Materials and Devices** III/V material integration, wide band gap, nanomagnetics, probabilistic, neuromorphic computing. Moderators: Yu-Hwa Lo (UCSD) & Peter Fischer (UCSC/LBNL) **Wireless** Precision navigation and timing, heterogeneous systems, cybersecurity, communication systems, wireless sensing, communications in complex/hostile environments, (underwater) acoustics, 6G+ Moderators: Peter Asbeck (UCSD) & Danijela Cabric (UCLA) **Electronic Design Automation (EDA)** Acceleration of design loop, tools, system technology co-optimization, path-finding. Tools for large scale heterogeneous integration. AI for EDA. Moderators: Andrew Kahng (UCSD) & Sheldon Tan (UCR)
3:50 pm	**Break –** people move back to the main room
4:00 pm	**Breakout Reporting** Breakout leads/moderators will provide a brief summary of main points discussed, and any point the group recommends be addressed during the next workshop.
4:45 pm	**Close**
5:00	**Networking Reception**

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Appendix: Organizing Team, Invited Speakers, and Workshop Attendees

First Name	Last Name	Title	Email Address	Institution	Workshop Role
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Jack	Kotovsky	Micro and Nano Technology Section Leader	kotovsky1@llnl.gov	LLNL	Organizer, Speaker
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